

## Design of Stochastic ALU Architecture and Analysis of Digital Computation in Dynamical Systems

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**Abstract:** In recent technologies, the floating point units will have high throughput in the arithmetic calculations, which have greater throughput in less time, and make easier to meet real time requirements. This can save power and extended battery life. These floating point units are followed by stochastic logic computation approach. Stochastic approach (SC) shown that the results about efficiency of the area in the low power system during the implementations of the hardware. The recent generation based applications has demand in high computational power with a minimal energy. SC is a computation format of digital system. This is followed by random bit streams for complex computations tasks, where smaller hardware is compared with conventional radix approaches. It is used by pseudo random numbers and analyzed by sequence of 0-1 binary format called stochastic numbers (SN). This paper followed a new technique of stochastic approach and analysis of digital computation with ALU design. In existing comparison, floating point ALU design is not implemented by stochastic approach. So, here proposed to implement stochastic ALU design. Where, arithmetic modules like addition, subtraction, multiplication are represented in the stochastic ALU design. Following module does not depend on other module. This modules are validated by VHDL stimulation and simulated in XILINX 14.2, finally area, power and delay comparison are shown.

**Keywords:** floating point numbers, random bit streams, stochastic numbers, and stochastic ALU design.

### I. Introduction

#### 1.1 Stochastic computing:

Stochastic computing is a digital approach to arithmetic computations. It has computational elements, where it is followed by real value numbers, and encoded as a Bernoulli sequence of length. A real value numbers include both rational and irrational numbers. Where, it is called complex numbers. These real numbers are pure standard format in mathematics. Here, the inputs are determined by the random bit streams. A standard logic unit of stochastic computing uses the process of pseudorandom bit streams. Simple low-power hardware was implemented by these arithmetic operations. Stochastic approach always has probabilities input. Stochastic circuit optimized to the conventional method. Therefore, it leads to reduction of cost. Stochastic circuits provide very high efficient power consumption. The inputs of random numbers are generated by stochastic number generators, which have significant portion of high accuracy. Benefits over these methods reduce fault tolerance, and implementing high clock rates. The inputs are always followed by random sequence of zeros and ones. Stochastic circuits are commonly has properties such as high error tolerance and very low power. So here analyzing computing tasks at low cost, where inputs are arranged in long random bit streams called stochastic numbers. In the floating point ALU with combination of universal logic gate. Here followed both arithmetic and logical operations, where it reduces delay and area. These frame work designing of combinational circuits with more correlated inputs demonstrate more efficient and accurate functions. Where, multiple instructions set are being followed by ALU design.

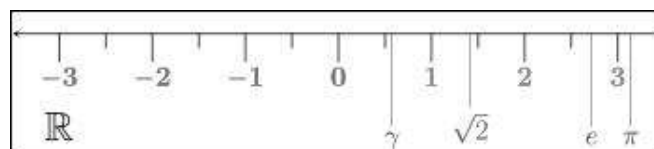


Fig. 1. Real numbers representation

The disadvantages of stochastic computing is low accuracy and long computing time .To overcome these draw backs here implementing stochastic ALU.

#### 1.2 Floating point ALU:

The floating point unit increases the range and precision values. The floating point unit has two parts; they are mantissa and exponent part. It is like a range of scientific notations. Floating point representations are

more expensive than the fixed point representations. The floating point ALU executes multiple instructions simultaneously. It is pipelined structure. The complexity of algorithm in FPGA is implemented by these floating point operations. Mainly floating points are followed by the precision range of values. Performing the operations of floating point ALU has main goals to achieve the accuracy in the signal computation process. The floating point describes the too small and large integer values. The fixed point representation has limited word size; it does not able to attain high resolution. To overcome these drawback of fixed The rest of the brief is as follows. In the section II, previous works on the stochastic computation and operations of floating ALU design is followed. Section III, discussed about proposed stochastic ALU architecture. Section IV The rest of the brief is as follows. In the section II, previous works on the stochastic computation and operations of floating ALU design is followed. Section III, discussed about proposed stochastic ALU architecture. Section IV, implementation of stochastic ALU design is discusses here. The results analysis and comparison are discussed in section V. section VI, shows the brief of the conclusion.

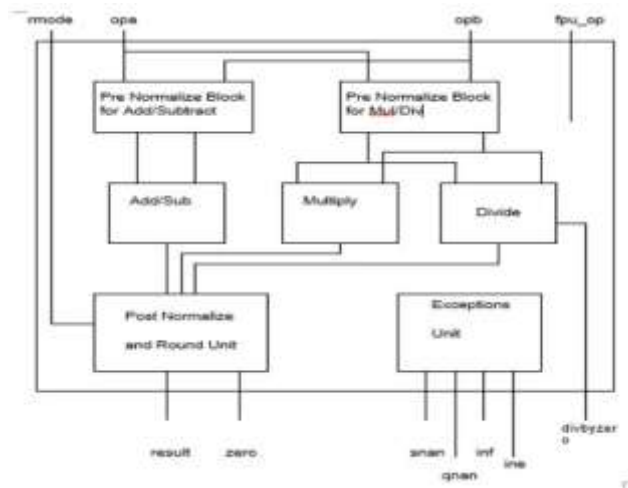
## II. Prior Work

### 2.1 Dynamical Systems:

This system is a mathematical formulization, that determines the time variant of ambient space. This system has a state representation. It is a collection of real numbers. It may be deterministic or stochastic. If only deterministic, which give time interval and then only one future state depends on the another current state. And if stochastic, which evaluates the state subject to random shocks.

### 2.2 Floating point ALU:

The floating point is an intensive application in various fields due to high dynamic range. It provides high precision and simplest way to implement every operation. Implementation of the arithmetic by hardware is very difficult. So the development of VLSI technology by FPGA has high integration, high performance. A large Range of numbers contains a fractional part, which responds to floating point representation, such as over flow representation.



**Fig. 2.** Floating point ALU design

### 2.3 Fixed Point:

When using pure integer arithmetic, It provides dramatic improvement, during the analysis of the floating point approach. The magnitude of each numbers ranges from 0 to 1 sequences. OFDM are especially many FFT and IFFT. Positive and negative numbers are readily implemented for productive and convenient format, flip flop and 2's complement. The FPU decide to use integer value during hardware operations and controlled by a specific integer values.

### 2.4 Formats:

These basic formats are based on the respective base and number of bits. The various binary formats encode the different number of bits.

**Table 1.** Binary Format Representation

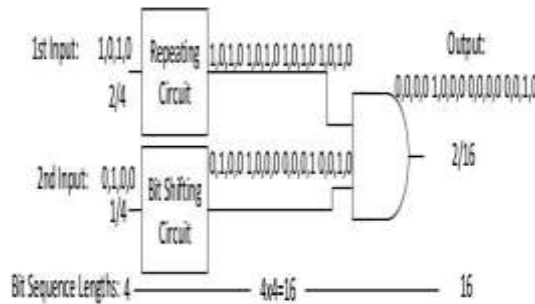
parameter → format name	b base	p (bits or digits)	emax
binary32	2	23+1 bits	+127
binary64	2	52+1 bits	+1023
binary128	2	112+1 bits	+16383
decimal64	10	16 digits	+384
decimal128	10	34 digits	+6144

**2.5 Single Precision:**

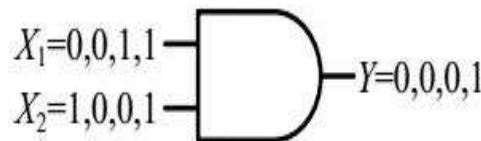
The layout of the single precision is followed by the three basic components is sign, exponent and mantissa.

**2.6 Stochastic Computing Approach:**

The main obstacles of the stochastic computing are the low accuracy and long computing times. The main importance of the stochastic computing is the reduction of the circuit size.

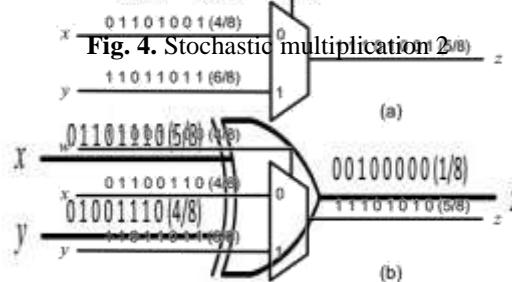


**Fig. 3.** Stochastic multiplication 1



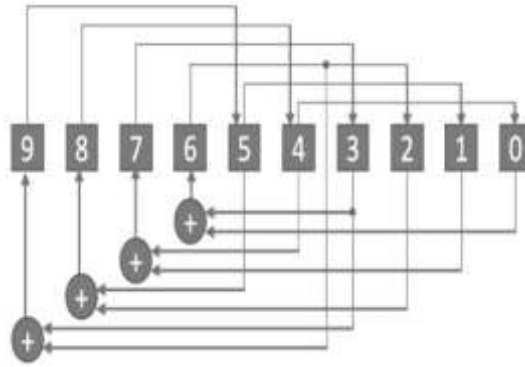
$$X_1 \times X_2 = Y$$

$$w \frac{1}{2} \times \frac{1}{2} = \frac{1}{4}$$



**Fig. 4.** Stochastic multiplication 2

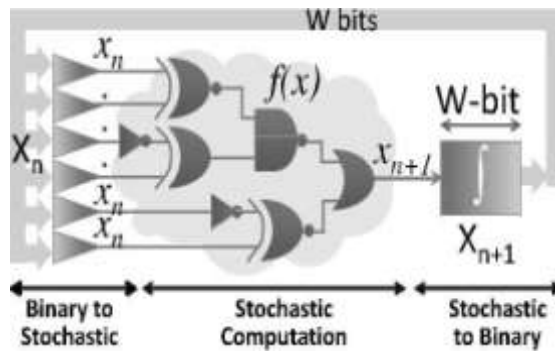
**Fig. 5.** Stochastic subtraction



**Fig. 6.** Stochastic addition

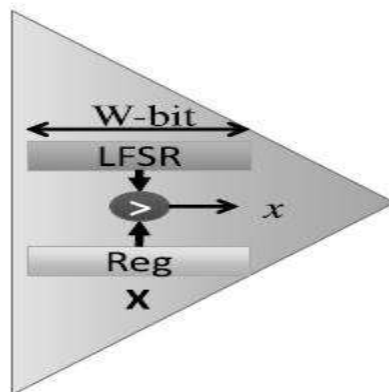
**2.7 Randomizer Based Feedback:**

If input bit streams are independently generated, which follows the conventional stochastic computation. Those error rates of outputs can be decreased. Then arrangement of random numbers in a stream is increased.



**Fig. 7.** Binary to stochastic computation

**2.8 Randomizer Circuit:**



**Fig. 8.** W-bit RNG

At each micro cycle, here random number is generated and compared to the register value. Where X is binary format and arranged in the register and W is the parameter controller which controls the values of resolution.

**2.9 LFSR:**

It is a linearity function of its existing states. The initial value of the LFSR is represented as seed, because the operations of the register are deterministic and it is used to develop an arrangement of bits that appear randomly pseudo random numbers and pseudo random –noise

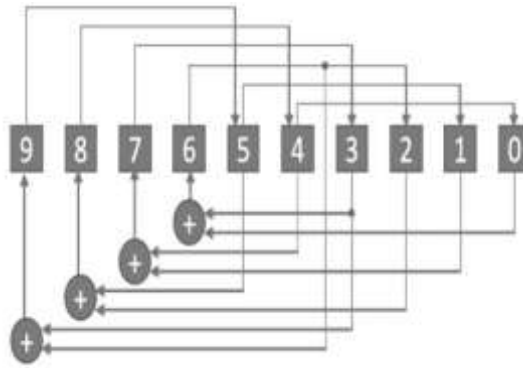


Fig. 9. LFSR

### III. Proposed System

The FPU is an arithmetic function using formulae arrangements of real numbers. Which, includes small and large real numbers that requires fast processing times. It is relative to the significand bit of these numbers. It is like a scientific notations. The floating point unit represent the fixed numbers of digits and different orders of magnitude. It involves intensive mathematical calculations. The way of following encoding numbers is usually in a string of digits. In scientific notation, these following values are scaled by power of 10. It lies between the range 1 and 10. It generally follows the conventional radix point. A signed integer has the magnitude of the integer value. For the derivation of floating point number, this significand bit is multiplied by base to the power of exponent. It is not followed by irrational values. It has base and prime factor. It does not represented in the memory, Which allow the format to have more values in the form of precision range, when memory is limited, It cannot store number with infinite precision. These format has to shows the accuracy results at different magnitudes. These must have relative accuracy. A fixed representation of these integer and fractional parts is in binary formats. A significand bit that has the rational values with an exponent part. Then the decimal point is arranged in a relative formation of the significand. For an exponent value, where the decimal point is fixed to the significand bit. The negative exponent values are represented here are very small. It is used to store and allow operations on approximation of real numbers. These real numbers contain the fractional part. The floating point unit are slower and less accuracy than the fixed point representation. The floating point number has an great deal of computation approach. Then microprocessors deals with a chip called floating point unit. The popular function of representing these numbers is called IEEE floating point standard.

#### 3.1 Operations of floating point unit:

The IEEE floating 754 format is based on the IEEE 754 binary floating point representation followed by the single and double precision formats. A real numbers are taken as input. First, the single precision values ranges from the rational numbers are converted into the 23 bits of single precision format. The range of single precision format is from -126 to 127. Where left side extreme gives the mantissa form of number. The exponent value is followed by the negative values, where it is used for bit wise comparison of floating point numbers. The smallest change in the FPU are called precision. The significand bit representation are determined by the accuracy. If arithmetic operations are followed by true form of results, when it is greater than the magnitude then it is called overflow. When it is less than the magnitude then it is called the underflow functions.

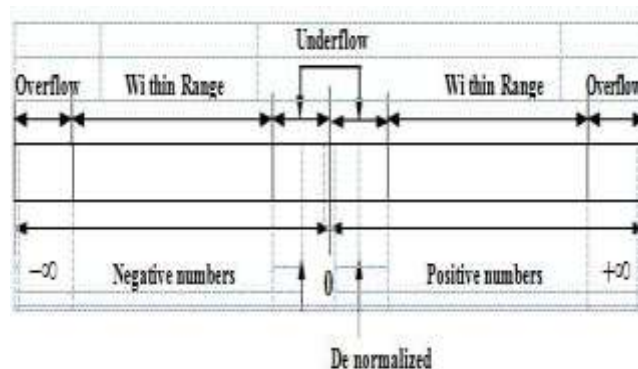
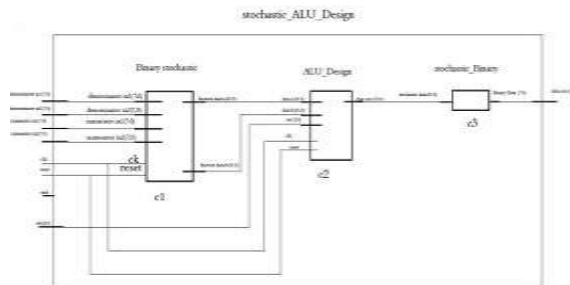


Fig. 10. Operations of floating point ALU

### 3.2 Proposed stochastic ALU design:

In the proposed floating point ALU design, they are two method follows as, Binary to stochastic, Stochastic to binary.



### 3.3 Random Number Generator:

Random numbers is the generation of sequences of numbers or symbols. It is mainly designed for cryptographically secure computational based method. It is the seed secret for sender and receiver, which generate the same set of numbers that automatically use as key.

For the purpose of security, The RNG generate numbers which attackers can't use the same numbers.

#### i) True Random Numbers:

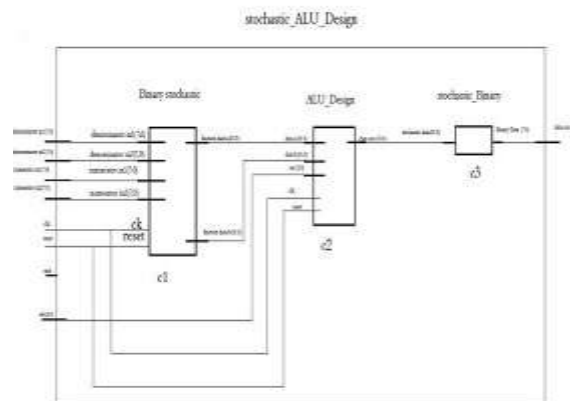
It is essentially used to predict the pure randomness from the universe. By the source of entropy only it is used to generate the true random numbers.

#### ii) Pseudorandom Numbers:

It is a seed value for a computer and respective coded values are generated for different numbers ,that appear to be random.

### 3.4 Stochastic ALU:

To design a combination of floating point ALU with stochastic approach, It follows the digital computation of stochastic approach. Then 0-1 sequences are implemented by the use of pseudo random numbers are called stochastic numbers. This paper introduced the analysis of dynamical digital computation and stochastic approach with ALU design. For the high resolution and accuracy. In existing comparison of floating point ALU is not implemented by stochastic approach, So here the proposed to implement a stochastic computing in ALU design.

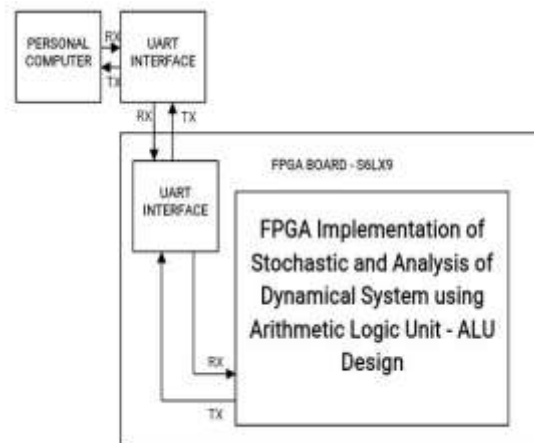


**Fig. 11.** Stochastic ALU design

In these methods inputs are taken as real number value. where in the form of fractional part with numerator and denominator. The 8 bit binary values are arranged in a long random bits. First, here all inputs are converted from real value to binary form. The binary form of inputs are arranged for stochastic operations. These stochastic outputs are send to the ALU design. Here stochastic ALU design follows the logical operations like AND, OR, XOR, NAND. And arithmetic operations like addition and subtraction. These stochastic inputs are arrived in the ALU design to these logical and arithmetic functions. Finally, outputs of stochastic ALU design again converted into the binary form of respective value. These respective values of ALU design are simulated by VHDL programming and synthesized in XILINX 14.2.

#### **IV. Hardware Implementation**

The binary input will provided through UART interface and it both ends are connected to the personal computer and FPGA lx 9 kit. In these FPGA lx 9 kit, where implementation of stochastic ALU is designed and VHDL code is dumped in it and stimulate the hardware output by VHDL coding.



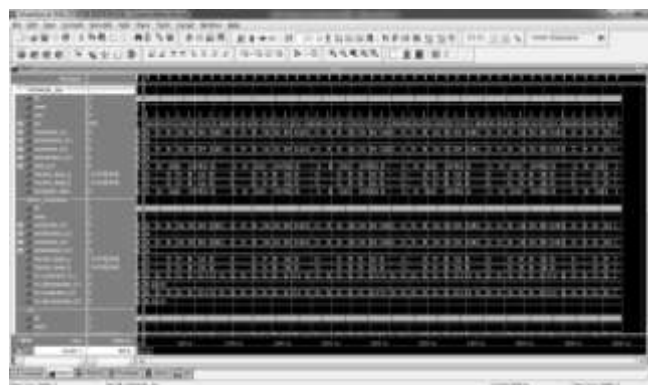
**Fig. 12.** Hardware implementation of stochastic ALU design

#### **V. Analysis Of Experimental Results**

Here, the analysis of stochastic ALU design shown that the comparative results of area, power, and timing report.



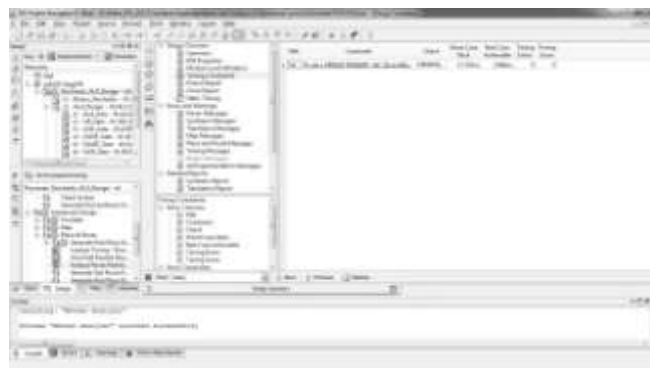
**Fig. 13.** RTL view of stochastic ALU design



**Fig. 14.** Simulation result



**Fig. 15.** Power report



**Fig. 16.** Timing report



**Fig. 17.** Area utilization

**Table 2.** Comparison Of Existing And Proposed System

contents	Existing System	Proposed System
Number of Slice Registers	227	0
Number of Slice LUT	17247	2437
Number of Occupied Slice	5913	798
Number of IOB	154	8
Total Power (mW)	36	19
Dynamic Power (nW)	-	6
Delay(ns)	-	4.118
Fanout effect	-	4.85



Finally, it shown the results of implementation of stochastic ALU design shown. Then the stochastic logics are used less power without the slice registers and reduction of delay and fan out effect.

Usage of total power = 0.019

Delay = 4.118 ns

Fan out effect =4.85

Here, the comparative results of existing and proposed system analyzes are shown in the section V.

## VI. Conclusion

This results simulates the better opportunities for noise generation and latency reduction. It involves various applications such as low-density parity –checker (LDPC) ,encoding filtering design. It is used in image processing, and look up table technique is exponentially used to speed up stochastic computation results in better energy consumption. The applicability of this method in emerging technologies including printed /flexible electronics for which low transistor is desired.

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